IN THE CLAIMS

Please amend the claims as follows:

Claims 1-2 (Canceled)

Claim 3 (Currently Amended): ~~The~~ An image processing apparatus ~~according to claim 1,~~ which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus comprising:

an input I/F memory configured to read pixels having a predetermined length, subject these pixels to buffering, and write these pixels in a SIMD type processor;

a SIMD type processor configured to perform batch processing of the pixels from said input I/F memory so as to provide batch processed pixels;

an output I/F memory configured to read the processed pixels, subject the processed pixels to buffering, and write the pixels in a predetermined output destination; and

a control unit configured to control read and/or write time of said input I/F memory and said output I/F memory,

wherein an effective number of pixels obtained by subtracting the number of peripheral pixels ~~referred to for said target pixel~~ from the number of batch processed pixels ~~batch processed by said SIMD type processor~~ is ~~multiples in~~ a multiple of the number of rows or columns of a dither matrix and an integer.

Claim 4 (Currently Amended): ~~The~~ An image processing apparatus ~~according to claim 1,~~ comprising:

an input I/F memory configured to read pixels having a predetermined length, subject these pixels to buffering, and write these pixels in a SIMD type processor;

a SIMD type processor configured to perform processing of the pixels from said input I/F memory to provide processed pixels;

an output I/F memory configured to read the processed pixels, subject the processed pixels to buffering, and write the pixels in a predetermined output destination; and

a control unit configured to control read and/or write time of said input I/F memory and said output I/F memory,

wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.

Claim 5 (Currently Amended): An image processing apparatus ~~which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus~~ comprising:

an input I/F memory ~~which reads~~ configured to read pixels having a predetermined length at a first speed, ~~subjects~~ subject these pixels to buffering, and ~~then writes these~~ write the pixels in a SIMD type processor at a second speed, the second speed being faster than the first speed ~~faster than when the pixel were read~~;

a SIMD type processor ~~which performs~~ configured to perform batch processing of the pixels written from said input I/F memory so as to provide batch processed pixels;

an output I/F memory ~~which reads~~ configured to read the batch processed pixels ~~batch processed by~~ from said SIMD type processor at a third speed, ~~subjects~~ subject the batch processed pixels to buffering, and ~~writes these~~ write the batch processed pixels in a predetermined output destination at a fourth speed, the fourth speed being slower than the third speed ~~slower than that of readout of said batch processed pixels~~; and

a control unit ~~which controls the~~ configured to control read and/or write ~~timing~~ time ~~and read and/or write speed~~ of said input I/F memory and said output I/F memory and control the first, second, third, and/or fourth speed.

Claim 6 (Currently Amended): The image processing apparatus according to claim 5, wherein said control unit controls the write and/or read ~~timing~~ time to thereby use said input I/F memory and output I/F memory a plurality of times.

Claim 7 (Canceled)

Claim 8 (Original): The image processing apparatus according to claim 5, wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.

Claim 9 (Currently Amended): An image processing apparatus ~~which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus~~ comprising:

an input I/F memory ~~which reads~~ configured to read pixels having a predetermined length at a first speed, ~~subjects these~~ subject the pixels to buffering, and ~~then writes these~~ write the pixels in a SIMD type processor at a second speed, the second speed being faster than the first speed ~~faster than when the pixels were read, and which has a capacity smaller than pixels batch processed by said SIMD type processor~~;

a SIMD type processor ~~which performs~~ configured to perform batch processing of the pixels written from said input I/F memory so as to provide batch processed pixels, the size of the batch processed pixels being larger than the size of the input I/F memory;

an output I/F memory ~~which reads~~ configured to read the batch processed pixels at a third speed ~~batch-processed by said SIMD-type processor~~, ~~subjects~~ subject the batch processed pixels to buffering, and ~~writes these~~ write the batch processed pixels in a predetermined output destination at a fourth speed, the fourth speed being slower than the third speed ~~slower than when the batch-processed pixels were read,~~ and the size of the batch processed pixels being larger than the size of the output I/F memory ~~which has a capacity smaller than pixels batch-processed by said SIMD-type processor~~; and

a control unit ~~which controls~~ configured to control the ~~write-and/or read~~ first and/or second speed ~~with respect said input I/F memory~~, and ~~the~~ write and/or read ~~timing~~ time ~~with respect~~ of said input I/F memory based on said first and/or second speed and the ~~capacity~~ size of said input I/F memory, and/or control the ~~write~~ third and/or ~~read~~ fourth speed ~~with respect said output I/F memory~~, and ~~the~~ write and/or read ~~timing with respect~~ time of said output I /F memory based on said third and/or fourth speed, and the ~~capacity~~ size of said output I/F memory.

Claim 10 (Currently Amended): The image processing apparatus according to claim 9, wherein said control unit controls the write and/or read ~~timing~~ time to thereby use said input I/F memory and output I/F memory a plurality of times.

Claim 11 (canceled)

Claim 12 (Original): The image processing apparatus according to claim 9, wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.